

WHAT IS CLAIMED IS:

- 1 1. A method of manufacturing a semiconductor device, the method comprising:
2 forming a lateral double-diffused metal oxide semiconductor (LDMOS) device in a
3 substrate, the LDMOS device including a drain;
4 forming a first guard ring around and proximate the drain of the LDMOS device; and
5 forming a second guard ring around the first guard ring.
- 1 2. The method according to Claim 1, wherein forming the first guard ring and forming the
2 second guard ring comprise forming a ring from a semiconductive material.
- 1 3. The method according to Claim 1, wherein forming the first guard ring comprises
2 forming a P+ base guard ring, and wherein forming the second guard ring comprises forming an
3 N+ collector guard ring.
- 1 4. The method according to Claim 3, wherein the first guard ring and the second guard ring
2 form a parasitic transistor, wherein the parasitic transistor electrically isolates the drain of the
3 LDMOS.
- 1 5. The method according to Claim 1, wherein forming the LDMOS device comprises
2 providing a substrate, forming an N+ buried layer in a top portion of the substrate, and
3 depositing a P-epitaxial layer over the N+ buried layer.
- 1 6. The method according to Claim 5, wherein depositing the P-epitaxial layer comprises
2 depositing about 9-10 μm of doped semiconductor material.

1 7. The method according to Claim 5, further comprising forming a deep N-well in the P-
2 epitaxial layer, wherein forming the first or second guard ring comprises forming the first or
3 second guard ring in the deep N-well.

1 8. The method according to Claim 7, wherein forming the deep N-well comprises forming
2 the deep N-well in the entire thickness of the P-epitaxial layer.

1 9. A method of manufacturing a lateral double-diffused metal oxide semiconductor
2 (LDMOS) device, the method comprising:
3 providing a substrate, the substrate comprising a first semiconductor type;
4 forming a first pad dielectric on a top surface of the substrate;
5 forming a buried layer in a top region of the substrate, the buried layer comprising a
6 second semiconductor type;
7 removing the first pad dielectric;
8 depositing a doped semiconductor material over the buried layer, the doped
9 semiconductor material being doped with the first semiconductor type;
10 forming a second pad dielectric over the doped semiconductor material;
11 doping a portion of the doped semiconductor material to form a deep well region, the
12 deep well region comprising an annular ring shape;
13 doping a portion of the doped semiconductor material to form at least one first high
14 voltage well region;
15 doping a portion of the doped semiconductor material to form a second high voltage well
16 region, the second high voltage well region comprising an annular shape disposed within a
17 central portion of the annular deep well region;
18 depositing a dielectric layer over the second pad dielectric;
19 patterning the dielectric layer;
20 removing exposed portions of the second pad dielectric;
21 forming field dielectric over portions of the second high voltage well region and the at
22 least one first high voltage well region using the dielectric layer as a mask;
23 removing the dielectric layer and remaining portions of the second pad dielectric;

24 forming a gate dielectric and gate of the LDMOS device over portions of the second high
25 voltage well region, the at least one first high voltage well region, and a portion of the field
26 dielectric;

27 simultaneously doping the annular deep well region, a portion of the second high voltage
28 well region and a portion of the at least one first high voltage well region with a dopant of the
29 second semiconductor type to form a first guard ring in the deep well region, a source of the
30 LDMOS device in the second high voltage well region, and a drain of the LDMOS device in the
31 at least one first high voltage well region; and

32 doping a portion of the annular second high voltage well region with a dopant of the first
33 semiconductor type to form a second guard ring in the second high voltage well region, the
34 second guard ring being formed in a central region of the first guard ring.

1 10. The method according to Claim 9, wherein the first semiconductor type comprises P-
2 type, wherein the second semiconductor type comprises N+, wherein the deep well region
3 comprises an N-well, wherein the at least one first high voltage well region comprises a high
4 voltage N-well (HVNW) region; wherein the second high voltage well region comprises a high
5 voltage P well (HVPW) region; wherein the dopant of the second semiconductor type comprises
6 N+; and wherein the dopant of the first semiconductor type comprises P+.

1 11. The method according to Claim 10, wherein depositing the P-doped semiconductor
2 material comprises depositing about 9-10 μm of P-epitaxial doped semiconductor material.

1 12. The method according to Claim 10, wherein forming the deep N-well region comprises
2 forming the deep N-well region in the entire thickness of the P-doped semiconductor material.

1 13. The method according to Claim 9, wherein forming the first pad dielectric comprises
2 forming a first pad oxide; wherein forming the second pad dielectric comprises forming a second
3 pad oxide; wherein depositing the dielectric layer comprises depositing a nitride layer; wherein
4 forming the field dielectric comprises forming a field oxide, and wherein forming the gate
5 dielectric comprises forming a gate oxide.

1 14. A semiconductor device, comprising:

2 a substrate;

3 a lateral double-diffused metal oxide semiconductor (LDMOS) device disposed in the
4 substrate, the LDMOS device including a drain;

5 a first guard ring disposed around and proximate the drain of the LDMOS device; and

6 a second guard ring disposed around the first guard ring.

1 15. The method according to Claim 14, wherein the first guard ring and the second guard ring
2 comprise a semiconductive material.

1 16. The semiconductor device according to Claim 14, wherein the first guard ring comprises
2 a P+ base guard ring, and wherein the second guard ring comprises an N+ collector guard ring.

1 17. The semiconductor device according to Claim 16, wherein the first guard ring and second
2 guard ring form a parasitic transistor, wherein the parasitic transistor electrically isolates the
3 drain of the LDMOS.

1 18. The semiconductor device according to Claim 14, wherein the semiconductor comprises
2 an N+ buried layer formed in a top portion of the substrate, and a P-epitaxial layer disposed over
3 the N+ buried layer.

1 19. The semiconductor device according to Claim 18, wherein the P-epitaxial layer
2 comprises about 9-10 μm of doped semiconductor material.

1 20. The semiconductor device according to Claim 18, further comprising a deep N-well
2 formed within the P-epitaxial layer, wherein the first or second guard ring is formed in the deep
3 N-well.

- 1 21. The semiconductor device according to Claim 20, wherein the deep N-well comprises the
2 entire thickness of the P-epitaxial layer.

1 22. A lateral double-diffused metal oxide semiconductor (LDMOS) device, comprising:
 2 a substrate, the substrate comprising a first semiconductor type;
 3 a buried layer formed in a top region of the substrate, the buried layer comprising a
 4 second semiconductor type;
 5 a doped semiconductor material disposed over the buried layer, the doped semiconductor
 6 material being doped with the first semiconductor type;
 7 a deep well region disposed within a portion of the doped semiconductor material, the
 8 deep well region comprising an annular ring shape and being doped with the first semiconductor
 9 type;
 10 at least one first high voltage well region formed within a portion of the doped
 11 semiconductor material;
 12 a second high voltage well region formed within a portion of the doped semiconductor
 13 material, the second high voltage well region comprising an annular shape disposed within a
 14 central portion of the annular deep well region;
 15 field dielectric disposed over portions of the at least one first high voltage well region and
 16 the second high voltage well region;
 17 a gate dielectric disposed over portions of the at least one first high voltage well region,
 18 the second high voltage well region, and a portion of the field dielectric;
 19 a gate of the LDMOS device disposed over the gate dielectric;
 20 a source of the LDMOS device formed in the second high voltage well region;
 21 a drain of the LDMOS device formed in the at least one first high voltage well region;
 22 a first guard ring formed in the annular deep well region; and

23 a second guard ring formed in the second high voltage well region, the second guard ring
24 being formed in a central region of the first guard ring.

1 23. The LDMOS device according to Claim 22, wherein the first semiconductor type
2 comprises P-type, wherein the second semiconductor type comprises N+, wherein the deep well
3 region comprises an N-well, wherein the at least one first high voltage well region comprises a
4 high voltage N-well (HVNW) region; wherein the second high voltage well region comprises a
5 high voltage P well (HVPW) region; wherein the dopant of the second semiconductor type
6 comprises N+, and wherein the dopant of the first semiconductor type comprises P+.

1 24. The LDMOS device according to Claim 22, wherein the P-doped semiconductor material
2 comprises about 9-10 μm of P-epitaxial doped semiconductor material.

1 25. The LDMOS device according to Claim 22, wherein the deep N-well region comprises
2 the entire thickness of the P-doped semiconductor material.

1 26. The LDMOS device according to Claim 22, wherein the field dielectric comprises a field
2 oxide, and wherein the gate dielectric comprises a gate oxide.